Figs. 25(a) and 25(b) illustrate asymmetrical I-V characteristics experimentally observed with an Ag nanocrystal memory device, the size of the device being W/L=3μm/9μm and the CHI being performed at V_{GS}=10V and $|V_{DS}|$=7V;

Figs. 26(a) and 26(b) illustrate an overprogramming problem experimentally observed in 2-bit-per cell nanocrystal memories, wherein devices have W/L=3μm/4μm, the "good cell" of Fig. 26(a) being written with V_{DS}=7V, V_{GS}=10V; the "overprogrammed cell" of Fig. 26(b) being written with V_{DS}=9V, V_{GS}=12, and wherein the solid symbols represent the I-V curves before CHI, and the hollow symbols represent the I-V curves after CHI;

Fig. 27 illustrates the effective mobility extracted from devices with different nanocrystals; and

DL ~~Fig. 28~~ Figs. 28 (a) - (d) illustrates deep depletion HFCV measurements for minority carrier lifetime estimation for Si, Ag, Au, and Pt.

Detailed Description of Preferred Embodiments of the Invention

[008] Turning now to a more detailed description of the invention, Fig. 1(a) illustrates in diagrammatic form a schematic of a memory cell 10 having discrete charge storage elements or nodes 12, which function as charge traps, embedded in an oxide layer 14, or gate dielectric, between a control gate electrode 16 and the surface 18 of a semiconductor substrate 20. Source and drain regions 22 and 24, respectively, are located on the substrate on opposite sides of a channel region 26, which is adjacent the location of the charge storage elements 12. The oxide material between the gate 16 and the charge storage elements 12 is referred to herein as the control oxide 28, while the oxide material between the elements 12 and the surface 18 is referred to as the tunnel oxide 30.

as a function of the electric field in tunnel oxide;

Fig. 5 illustrates band diagrams illustrating the design considerations with work function engineering;

Fig. 6 illustrates F-N tunneling transmission coefficients through SiO_2 barrier from metals with different work functions;

Fig. 7 is a band diagram illustrating the necessity of tuning control gate work function in order to achieve effective write/erase operations in the F-N tunneling regime;

Fig. 8 illustrates a process sequence for metal nanocrystal formation;

Fig. 9 is a schematic illustration of the driving forces in the self-assembly process of Fig. 8;

Figs. 10(a)-(d) illustrate the effect of initial film thickness on Au nanocrystal formation;

Fig. 11 illustrates the effect of annealing temperature on W nanocrystal formation;

Figs. 12(a) to 12(h) illustrate a process flow for fabricating metal nanocrystal memory devices;

Fig. 13 illustrates the density and size distribution of Ag, Au and Pt nanocrystals;

Figs. 14(a)-(d) illustrate the write/erase characteristics of nanocrystal memory devices by F-N tunneling;

Fig. 15

DL ~~Figs. 15(a) and 15(b)~~ illustrate the gate current under erase and write conditions, respectively, for the samples shown in Fig. 13;

Fig. 16 illustrates a write operation by CHI for devices with different nanocrystals;

Fig. 17 illustrates the threshold voltage shift caused by local charging in a split-gate MOSFET;